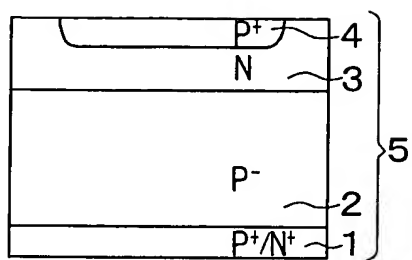
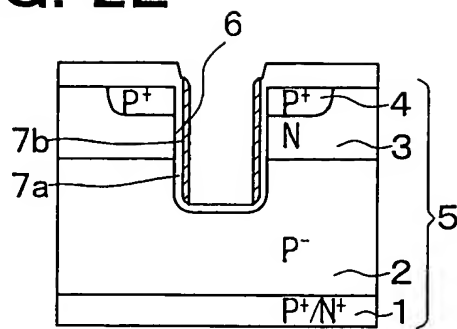


A cross-sectional view of a semiconductor device. The device is built on a substrate (1) with a  $P^+/N^+$  layer. A central channel region (2) is defined by a  $P^-$  layer. The channel is flanked by side regions (3) containing  $N$  dopants. The top of the device is covered by a layer (4) with  $P^+$  regions. A central region (5) is defined by a  $P^-$  layer. The device is surrounded by a passivation layer (6). The channel is defined by a  $P^-$  layer (7e) and a  $P^+$  layer (7d). The side regions are defined by a  $P^-$  layer (7b) and a  $P^+$  layer (7c). The top of the device is covered by a layer (7a) with a  $P^+$  region (7f). The device is surrounded by a passivation layer (7g). The channel is defined by a  $P^-$  layer (7e) and a  $P^+$  layer (7d). The side regions are defined by a  $P^-$  layer (7b) and a  $P^+$  layer (7c). The top of the device is covered by a layer (7a) with a  $P^+$  region (7f). The device is surrounded by a passivation layer (7g). The channel is defined by a  $P^-$  layer (7e) and a  $P^+$  layer (7d). The side regions are defined by a  $P^-$  layer (7b) and a  $P^+$  layer (7c). The top of the device is covered by a layer (7a) with a  $P^+$  region (7f). The device is surrounded by a passivation layer (7g).

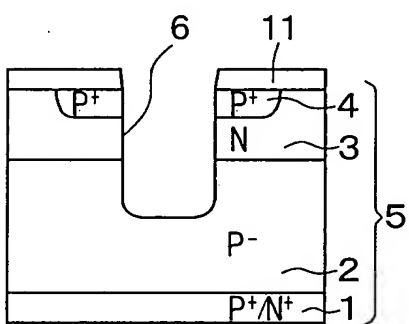
**FIG. 2A**



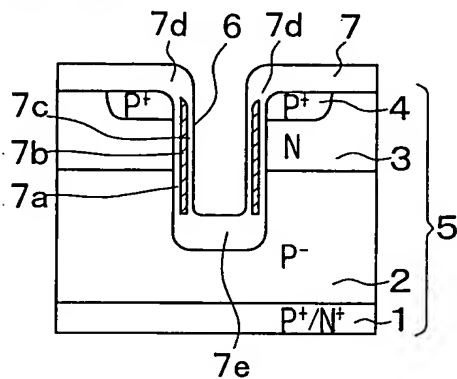
**FIG. 2E**



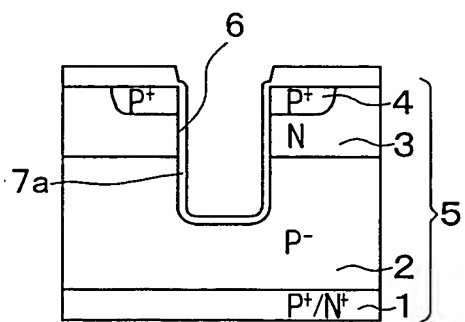
**FIG. 2B**



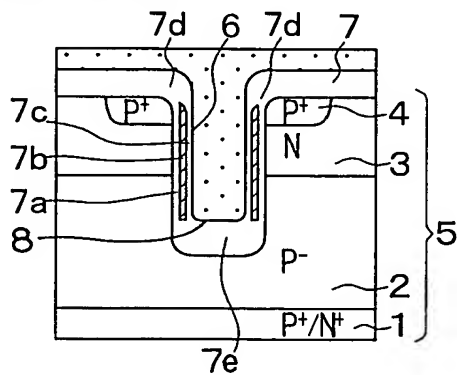
**FIG. 2F**



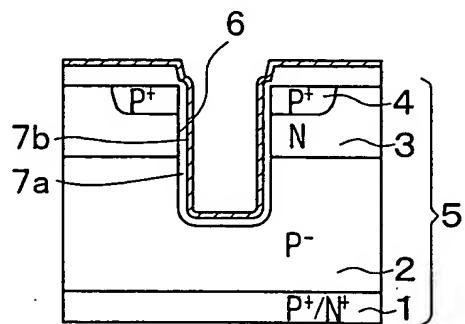
**FIG. 2C**



**FIG. 2G**



**FIG. 2D**



**FIG. 2H**

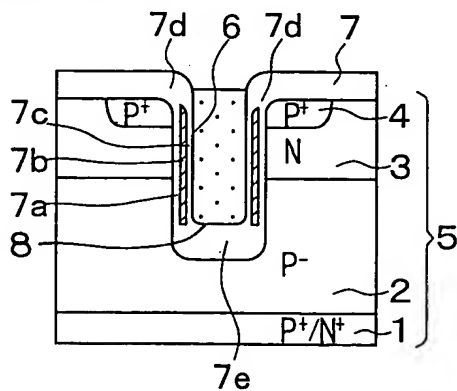


FIG. 3

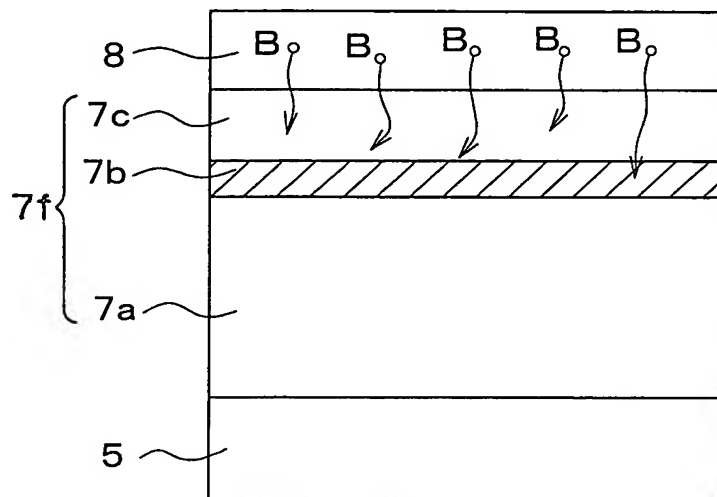


FIG. 4

